Bluetooth Module Specification

Model: TL-QCC-5C

Version: V0.2

1. Description

TL-QCC-5C is the latest generation of Bluetooth Module. It provides highest level of integration With integrated 2.4GHz radio, DSP, Power management, battery Charger, stereo audio CODEC, and antenna and can be designed for mono and stereo audio applications.

TL-QCC-5C has also support the latest Bluetooth v5.2 BR/EDR and BLE Dual mode standard and support for secure Simple pairing.

2. Features

2.1 Bluetooth Profiles

- Bluetooth v5.2 BR/EDR and BLE Dual mode specification support
- BLE v5.2（BLE Speed 2Mbps）
- HFP v
- HSP v
- A2DP v
- AVRCP v
- SPP v
- HOGP v
- HID v
- QTIL's proximity pairing and QTIL's proximity connection
- Wired/wireless mono headsets/headphones
- Qualcomm TrueWireless™ stereo earbuds

2.2 General features

- Qualified to Bluetooth v5.2 specification
- 120 MHz Qualcomm® Kalimba™ audio DSP
- 32 MHz Developer Processor for applications
- Firmware Processor for system
- Flexible QSPI flash programmable platform
- High-performance 24-bit audio interface
- Digital and analog microphone interfaces
- Flexible PIO controller and LED pins with PWM support
- Serial interfaces: UART, Bit Serializer (I²C/SPI), USB 2.0
- Advanced audio algorithms
- Active Noise Cancellation: Hybrid, Feedforward, and Feedback modes, using Digital or Analog Mics, enabled using license keys available from Qualcomm®

◆ Qualcomm® aptX™ and aptX HD Audio

◆ 1 or 2 mic Qualcomm® cVc™ headset speech processing

◆ Integrated PMU: Dual SMPS for system/digital circuits, Integrated Li-ion battery charger

2.3 Application subsystem

◆ Dual-core application subsystem 32 MHz operation

◆ 32-bit Firmware Processor (reserved for system use) executes:

- □ Bluetooth upper stack
- □ Profiles
- □ House-keeping code

◆ 32-bit Developer Processor executes: Developer applications

◆ 32 Mb flash memory

◆ On-chip caches per core enable optimized performance and power consumption

2.4 Bluetooth subsystem

◆ Qualified to Bluetooth v5.2 specification including 2 Mbps Bluetooth Low Energy

◆ Single ended antenna connection with on-chip balun and Tx/Rx switch

◆ Bluetooth, Bluetooth Low Energy, and mixed topologies supported

◆ Class 1 support

3. Electrical Characteristics

Recommended operating conditions

	Min	Typ	Max	Unit
Storage temperature	-40	25	85	℃
Operating temperature	-40	25	85	℃
Charger temperature range	-10	25	85	℃
VDD_BAT	2.8	3.7	4.6	V
VDD_CHG	4.75	5.0	6.50	V
VDD_IO	1.7	1.8	3.6	V
VDD_USB	2.8	3.3	3.5	V
LED Open drain current	-	-	50	mA
Charger Current(Internal)	2	-	200	mA
Charger Current(External)	200	-	1800	mA
Sco Current	-	-	TBD	mA
Stream Current	-	-	TBD	mA
Idle Current	-	-	TBD	mA
Off Current	-	-	TBD	uA

4. Specifications

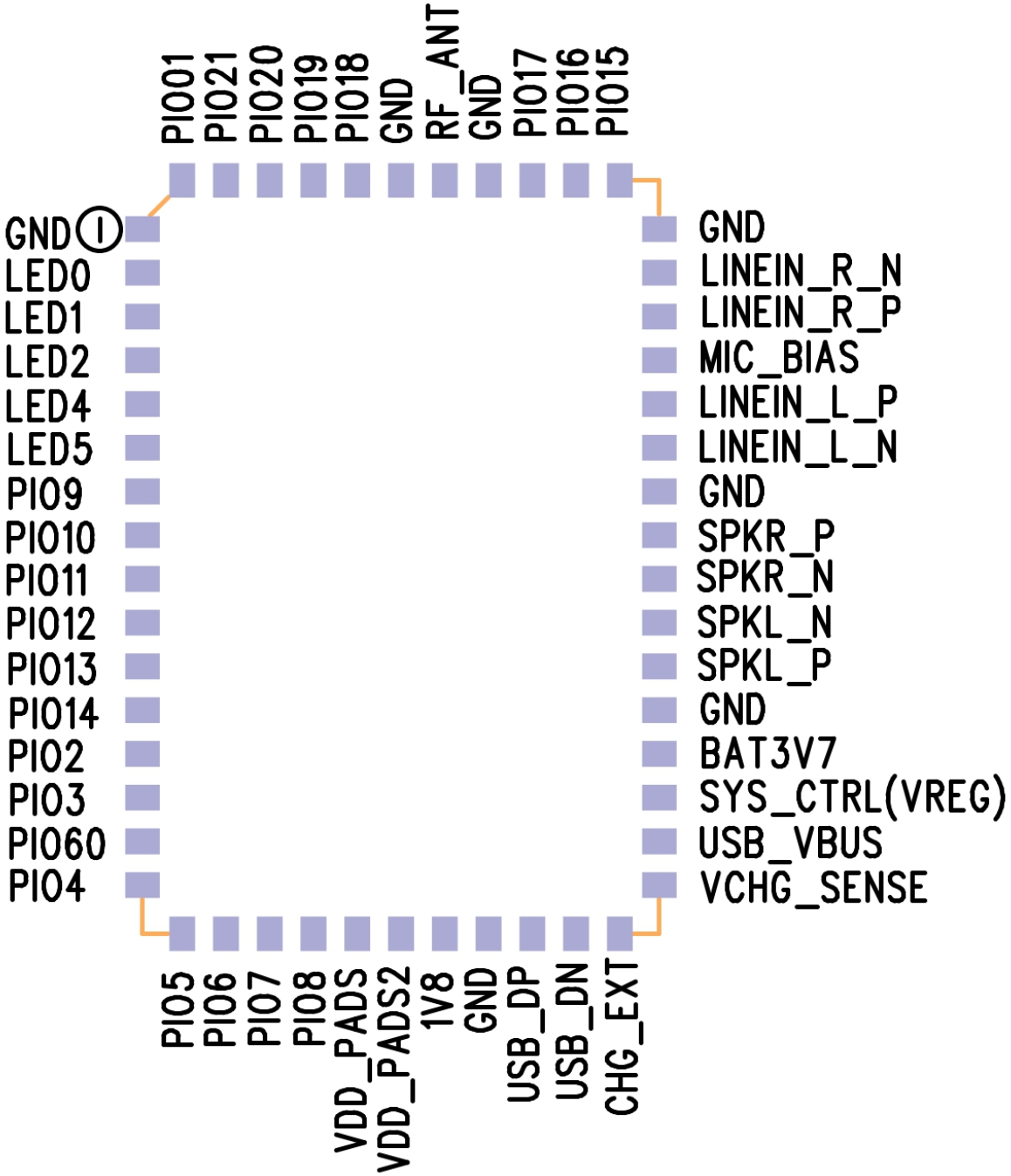
General Specifications

General		
Chips	QCC3040 VFBGA(earbuds), QCC3044 VFBGA(headsets)	
Bluetooth specification	v5.2	
Frequency Range	2402～2480MHz	
Modulation mode	GFSK, π/4-DQPSK, 8DPSK	
Maximum RF Transmit Power	GFSK	13dBm
	π/4-DQPSK	10dBm
	8DPSK	10dBm
	Low Energy	10dBm
Receive Sensitivity	GFSK	-95dBm
	π/4-DQPSK	-95dBm
	8DPSK	-88dBm
	Low Energy	-98dBm
Operating Voltage	Battery: 2.8V ~ 4.6V, Charger: 5.0V	
Host Interface	PIO, LED, AIO, USB, UART, I2C, SPI	
Audio Interface	SPK&MIC, PCM, I2S, SPDIF, USB	
Flash Memory Size	32Mbits	
Dimension	17.5mm(L) x 12mm(W) x 1.8mm(H)	

Audio features	Min	Typ	Max	Unit
ADC Output Sample Width	-	-	24	Bits
ADC Output Sample Rate, Fsample	8	-	96	kHz
ADC Input level	-	-	2.4	V_{pk-pk}
ADC Input impedance	20(0 dB to 24 dB analog gain)			kΩ
	10(27 dB to 39 dB analog gain)			kΩ
ADC Digital Gain	-24	-	21.5	dB
ADC Analog Gain	0	-	39	dB
ADC SNR	-	99.4	-	dB
ADC THD+N	-	95.5	-	dB
ADC Stereo separation (crosstalk)	80	-	-	dB
DAC Input Sample Width	-	-	24	Bits
DAC Input Sample Rate, Fsample	8	-	192	kHz
DAC Output Power	-	-	30	mW

DAC Digital Gain	-24	0	21.5	dB
DAC SNR	-	99.3	-	dB
DAC THD+N	-	93.5	-	dB
DAC Stereo separation (crosstalk)	80	-	-	dB

5. Device Terminal Functions

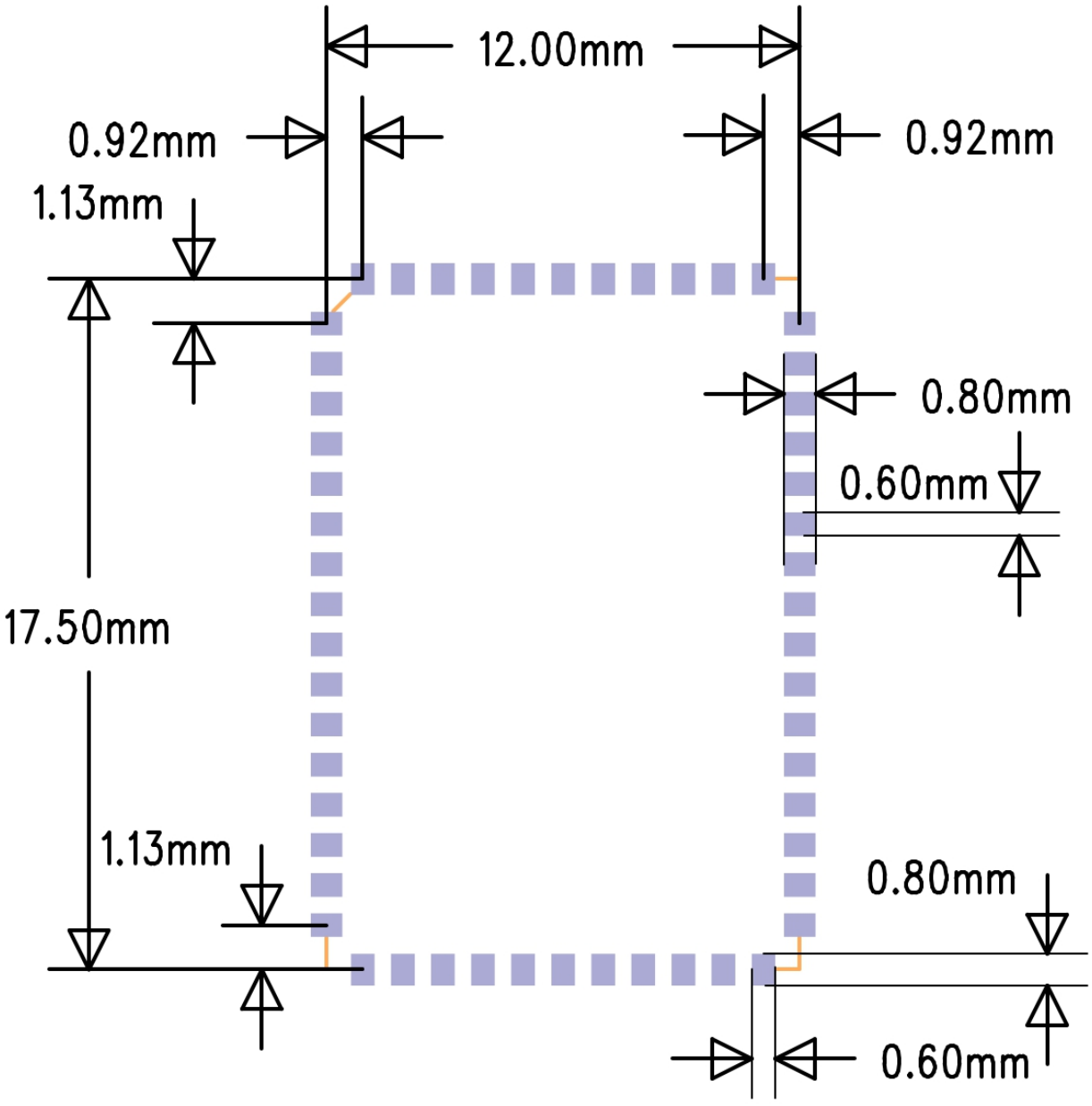


Pin NO.	Name	Level	Function and Description
1	GND	Ground	Ground connection
2	AIO[0]/LED[0]	VDD_BYP	General-purpose analog/digital input. ■ open drain LED output.
3	AIO[1]/LED[1]	VDD_BYP	General-purpose analog/digital input. ■ open drain LED output.
4	AIO[2]/LED[2]	VDD_BYP	General-purpose analog/digital input. ■ open drain LED output.
5	AIO[4]/LED[4]	VDD_BYP	General-purpose analog/digital input. ■ open drain LED output.
6	AIO[5]/LED[5]	VDD_BYP	General-purpose analog/digital input. ■ open drain LED output.
7	PIO9	VDD_PADS_2	Programmable I/O line 9.
8	PIO10	VDD_PADS_2	Programmable I/O line 10.
9	PIO11	VDD_PADS_2	Programmable I/O line 11.
10	PIO12	VDD_PADS_2	Programmable I/O line 12.
11	PIO13	VDD_PADS_2	Programmable I/O line 13.
12	PIO14	VDD_PADS_2	Programmable I/O line 14.
13	PIO2	VDD_PADS	Programmable I/O line 2. ■ TBR_MISO[3]
14	PIO3	VDD_PADS	Programmable I/O line 3. ■ TBR_MISO[2]
15	PIO60	VDD_PADS	Programmable I/O line 60.
16	PIO4	VDD_PADS	Programmable I/O line 4. ■ TBR_MOSI[1]
17	PIO5	VDD_PADS	Programmable I/O line 5. ■ TBR_MISO[1]
18	PIO6	VDD_PADS	Programmable I/O line 6. ■ TBR_MOSI[0]
19	PIO7	VDD_PADS	Programmable I/O line 7. ■ TBR_MISO[0]
20	PIO8	VDD_PADS	Programmable I/O line 8. ■ TBR_CLK
21	VDD_PADS	1.8/3.3V	PIO supply input
22	VDD_PADS2	1.8/3.3V	PIO supply input
23	1V8	1.8V	1.8 V supply output
24	GND	Ground	Ground connection
25	USB_DP	VDD_BYP	USB Full Speed device D- I/O. IEC-61000-4-2 (device level) ESD Protection
26	USB_DN	VDD_BYP	USB Full Speed device D+ I/O. IEC-61000-4-2 (device level) ESD Protection
27	CHG_EXT	VCHG	External charger transistor current control. Connect to base of external charger transistor

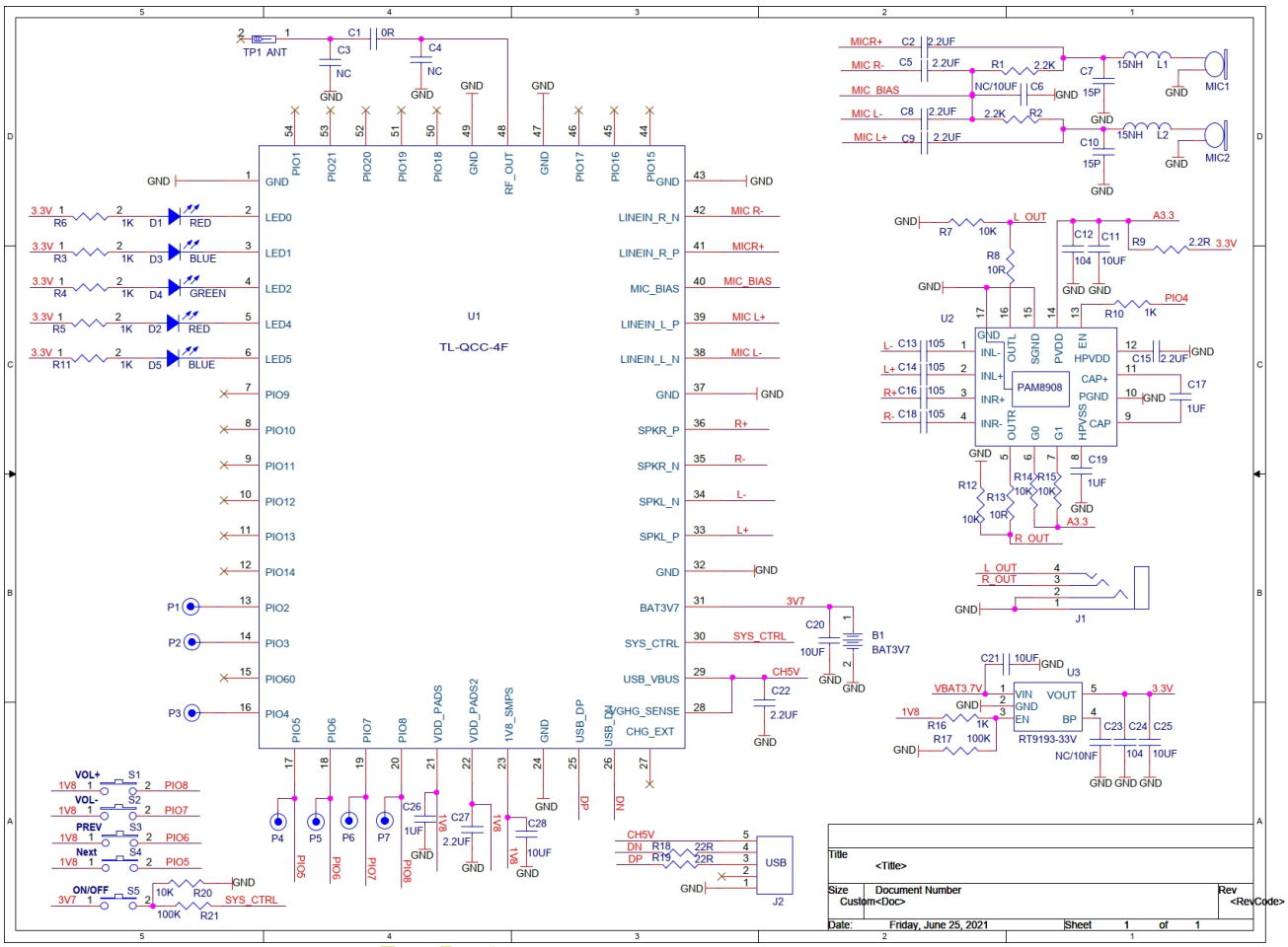
			as per application schematic.
28	VCHG_SENSE	VCHG	Charger input sense pin after external mode sense-resistor. High impedance. NOTE If using internal charger or no charger, connect VCHG_SENSE direct to VCHG.
29	USB_VBUS	4.75V~6.50V	Charger input to Bypass regulator.
30	SYS_CTRL	VBAT	Typically connected to an ON/OFF push button. If power is present from the battery and/or charger, and software has placed the device in the OFF or DORMANT state, a button press boots the device. Also usable as a digital input in normal operation. No pull. ■ Additional function: PIO[0] input only
31	BAT3V7	2.8V ~ 4.6V	Battery voltage input.
32	GND	Ground	Ground connection
33	SPKL_P	Analog	Headphone/speaker differential left output, positive. ■ Differential left line output, positive
34	SPKL_N	Analog	Headphone/speaker differential left output, negative. ■ Differential left line output, negative
35	SPKR_N	Analog	Headphone/speaker differential right output, negative. ■ Differential right line output, negative. NOTE: QCC3040 NC
36	SPKR_P	Analog	Headphone/speaker differential right output, positive. ■ Differential right line output, positive. NOTE: QCC3040 NC
37	GND	Ground	Ground connection
38	LINE_L_N	Analog	Microphone differential 1 input, negative. ■ Differential audio line input left, negative
39	LINE_L_P	Analog	Microphone differential 1 input, positive. ■ Differential audio line input left, positive
40	MIC_BIAS	1.8V	Mic bias output.
41	LINE_R_P	Analog	Microphone differential 2 input, positive. ■ Differential audio line input right, positive
42	LINE_R_N	Analog	Microphone differential 2 input, negative. ■ Differential audio line input right, negative
43	GND	Ground	Ground connection
44	PIO15	VDD_PADS	Programmable I/O line 15. ■ MCLK_OUT
45	PIO16	VDD_PADS	Programmable I/O line 16. ■ PCM_CLK
46	PIO17	VDD_PADS	Programmable I/O line 17.

			■ PCM_SYNC
47	GND	Ground	Ground connection
48	RF_ANT		Bluetooth 50Ω transmitter output / receiver input.
49	GND	Ground	Ground connection
50	PIO18	VDD_PADS	Programmable I/O line 18. ■ PCM_DOUT[0]
51	PIO19	VDD_PADS	Programmable I/O line 19. ■ PCM_DIN[0]
52	PIO20	VDD_PADS	Programmable I/O line 20. ■ PCM_DOUT[1]
53	PIO21	VDD_PADS	Programmable I/O line 21. ■ PCM_DOUT[2]
54	PIO1	VDD_PADS	Automatically defaults to RESET# mode when the device is unpowered, or in off modes. Reconfigurable as a PIO after boot. ■ Programmable I/O line 1

6. Package Dimensions

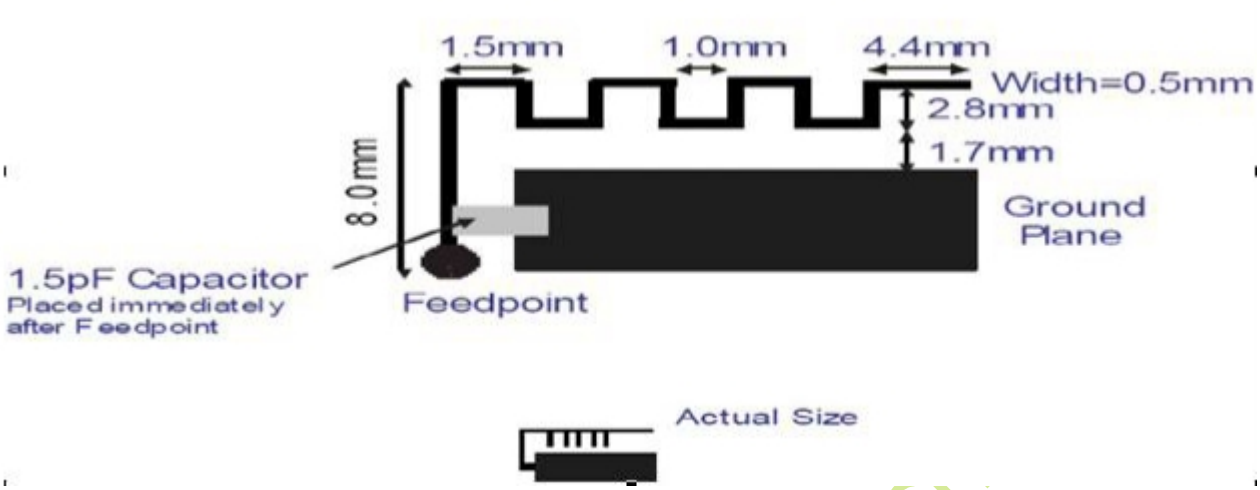


7. Example Application Schematic

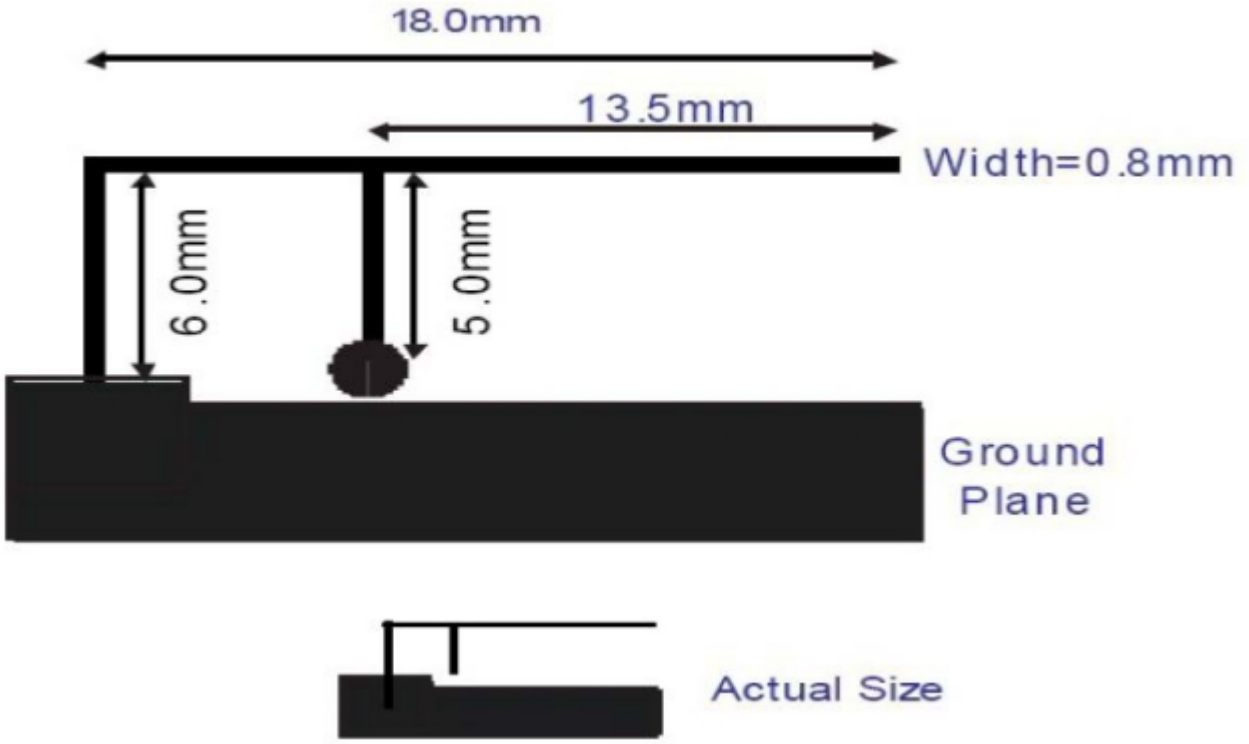


8. PCB Antenna Example

8.1 Meander Antenna



8.2 Inverted-F-Antenna



9. Layout Guidelines

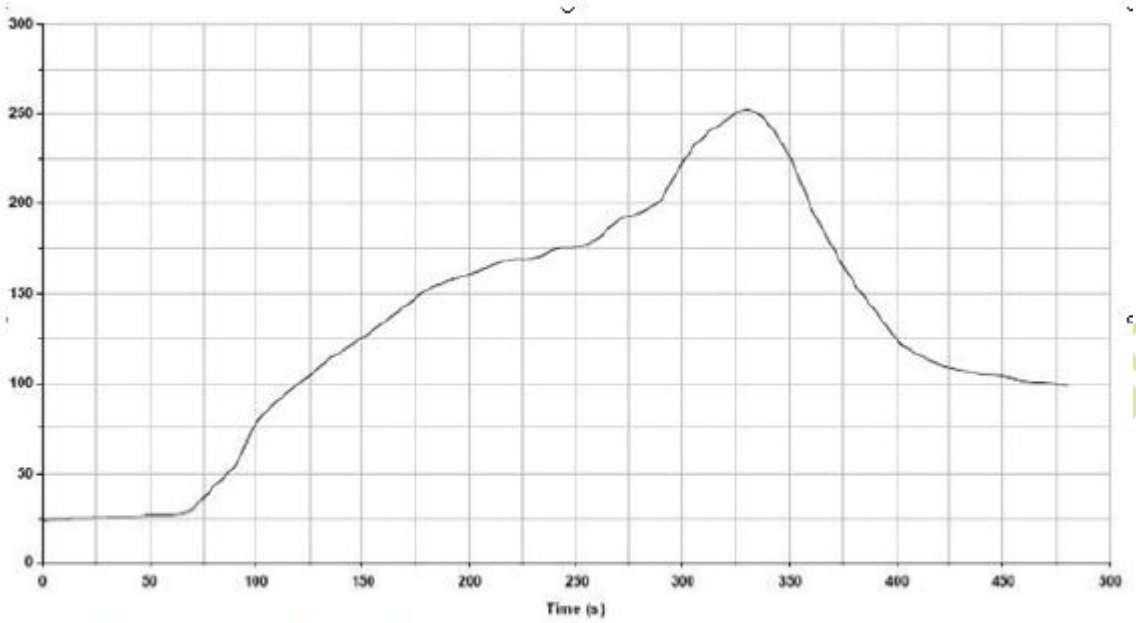
9.1 Audio Layout

Route audio lines as differential pairs. The positive and negative signals should run parallel and close to each other until they are converted to single-ended signals. Use dedicated audio ground plane for entire audio section.

9.2 Antenna Design

Do not place GND plane or any metal directly under the antenna of TL-BC6-04. To avoid any excess parasitic capacitance in the antenna feed line caused by the RF test pin on the bottom side of the module, the area underneath the RF test pin should also be left free from copper. Any metal in close proximity of the antenna will have an effect on the antenna performance. Thus any metal should be placed as far from the antenna as possible. The module should be placed to an edge of the PCB.

10. Recommended Reflow Soldering Temperature



Key features of the profile:

-Initial Ramp=1-2.5℃/sec to 175℃ equilibrium
-Equilibrium time=60 to 80 seconds
-Ramp to Maximum temperature (250℃)=3℃/sec Max
-Time above liquidus temperature(217℃): 45 - 90 seconds
-Device absolute maximum reflow temperature: 250℃